



The Design of Low Noise Oscillators

Ali Hajimiri, Thomas H Lee

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It is hardly a revelation to note that wireless and mobile communications have grown tremendously during the last few years. This growth has placed stringent requirements on channel spacing and, by implication, on the phase noise of oscillators. Compounding the challenge has been a recent drive toward implementations of transceivers in CMOS, whose inferior $1/f$ noise performance has usually been thought to disqualify it from use in all but the lowest-performance oscillators. Low noise oscillators are also highly desired in the digital world, of course. The continued drive toward higher clock frequencies translates into a demand for ever-decreasing jitter. Clearly, there is a need for a deep understanding of the fundamental mechanisms governing the process by which device, substrate, and supply noise turn into jitter and phase noise. Existing models generally offer only qualitative insights, however, and it has not always been clear why they are not quantitatively correct.

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